AMENDMENTS TO THE CLAIMS

1. (currently amended) A method for fabricating non-volatile memory cells, the method comprising:

forming a plurality of pillars ~~pillar~~ of silicon vertically extending above a substrate, each pair of pillars forming a trench;

implanting a drain region in a top of ~~the~~ each pillar;

implanting ~~first and second~~ source regions in the substrate under each trench ~~and adjacent to the pillar, wherein the first and second source regions are located on opposite sides of the pillar~~;

depositing a gate oxide on at least vertical sides of ~~the~~ each pillar ~~facing the first and second source regions~~;

forming floating gates adjacent to and on opposite sides of ~~the~~ each pillar;

forming first and second control gates as a single unit in each trench and insulated from the floating gates ~~and~~ located on opposite sides of the trench ~~pillar~~; and

forming a wordline in each trench such that the wordline is structurally separate from but connected to the first and second control gates, the wordline parallel to and between the first and second control gates.

2. (Original) The method of claim 1 wherein the floating gates are fabricated using polysilicon.

3. (Original) The method of claim 1 wherein the control gates are fabricated using polysilicon and silicide.

4 – 6 (canceled)

7. (currently amended) A method for fabricating a memory array, the method comprising:

etching a first series of parallel trenches in a substrate;

filling the first series of parallel trenches with oxide;

etching a second series of parallel trenches in the substrate, wherein the second series of parallel trenches are perpendicular to the first series of parallel trenches such that a plurality of substrate material pillars are formed and separated in a first direction by the oxide and a second direction by the second trenches;

implanting source regions at a bottom of the second series of parallel trenches;

implanting drain regions in the top of the pillars;

fabricating floating gates in the second series of parallel trenches and insulated from the pillars;

fabricating a pair of control gates in each of the second series of parallel trenches and insulated from the floating gates, the pair of control gates formed as a single unit along the sides and bottom of each of the second series of parallel trenches; and

fabricating a wordline parallel to and between ~~the~~ each pair of control gates, the wordline being structurally separate from but connected to each pair of control gates.

8. (Original) The method of claim 7 wherein the floating gates and control gates comprise polysilicon.

9. (Original) The method of claim 7 wherein the control gates comprise a layer of polysilicon and a layer of tungsten.

10. (Original) The method of claim 7 further comprises:

fabricating vertically extending source contacts in electrical contact with the source regions;

fabricating conductive sources lines in electrical contact with the source contacts;

fabricating vertically extending drain contacts in electrical contact with the drain regions; and

fabricating conductive drain lines in electrical contact with the drain contacts.

11. (currently amended) A method for fabricating a memory array, the method comprising:

depositing a layer of nitride on a substrate;

etching a first series of parallel trenches in the layer of nitride;

filling the first series of parallel trenches with oxide by depositing a layer of thin oxide;

planarizing the layer of thin oxide with a chemical mechanical planarization process to remove the layer of thin oxide and leave the first series of parallel trenches filled with oxide;

etching a second series of parallel trenches in the substrate, wherein the second series of parallel trenches are perpendicular to the first series of parallel trenches such that a plurality of

substrate material pillars are formed and separated in a first direction by the oxide and a second direction by the second trenches;

implanting source regions at a bottom of the second parallel trenches;

implanting drain regions in the top of the pillars;

fabricating floating gates in the second trenches and insulated from the pillars;

fabricating a pair of control gates in each of the second trenches and insulated from the floating gates; and

fabricating a wordline parallel to and between ~~the~~ each pair of control gates, the wordline being structurally separate from but connected to each pair of control gates.

12. (Original) The method of claim 11 and further including depositing a layer of oxide on the substrate prior to depositing the layer of nitride.